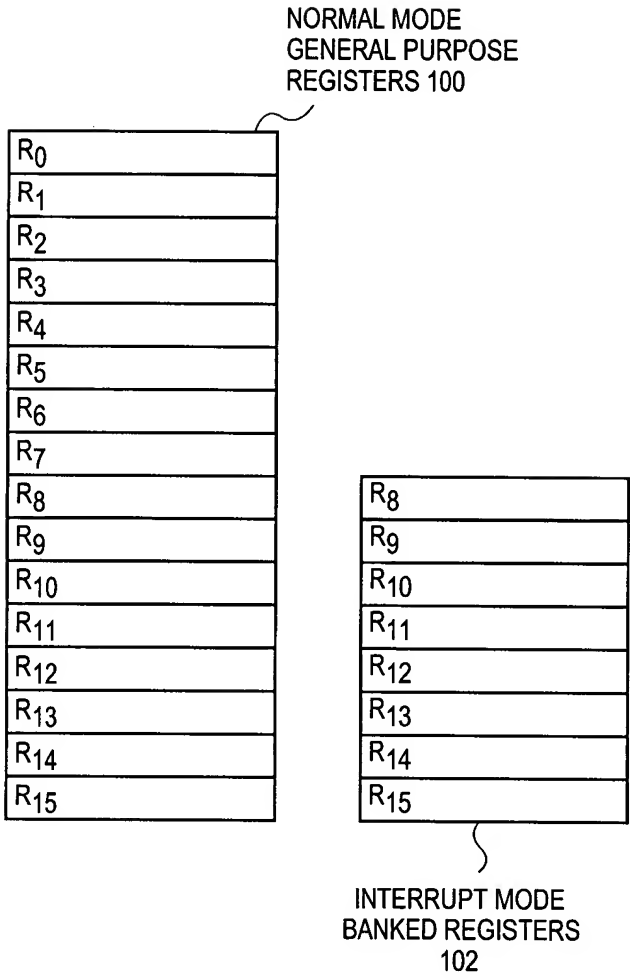

FIG. 1
(PRIOR ART)

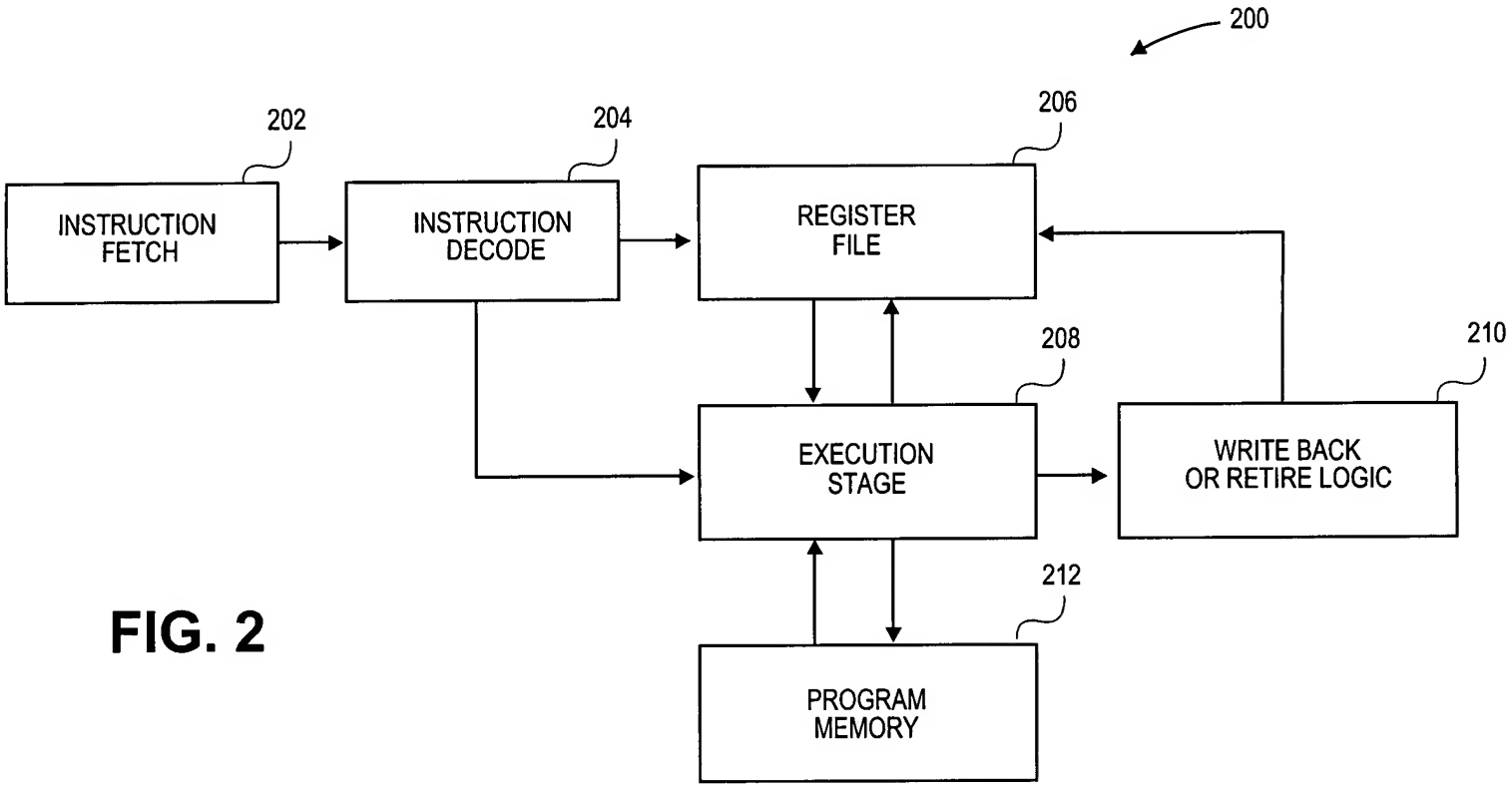
200
202
INSTRUCTION FETCH
204
INSTRUCTION DECODE
206
REGISTER FILE
208
EXECUTION STAGE
210
WRITE BACK OR RETIRE LOGIC
212
PROGRAM MEMORY

FIG. 2

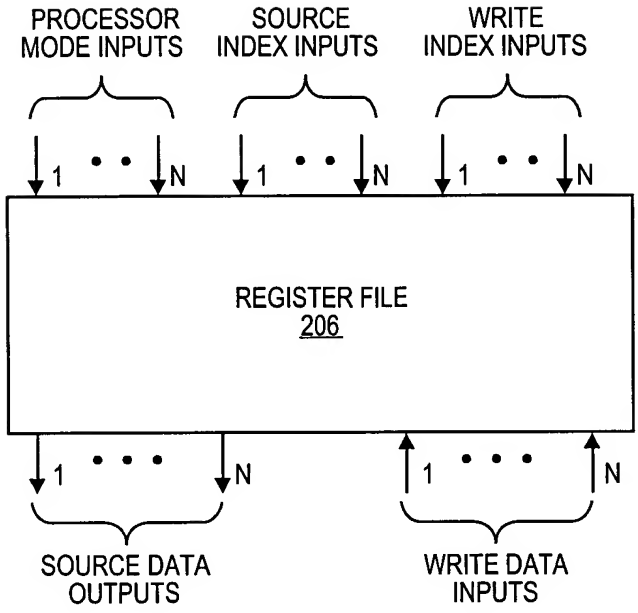
PROCESSOR MODE INPUTS
SOURCE INDEX INPUTS
WRITE INDEX INPUTS
1
N
1
N
1
N
REGISTER FILE
206
1
N
1
N
SOURCE DATA OUTPUTS
WRITE DATA INPUTS

FIG. 3

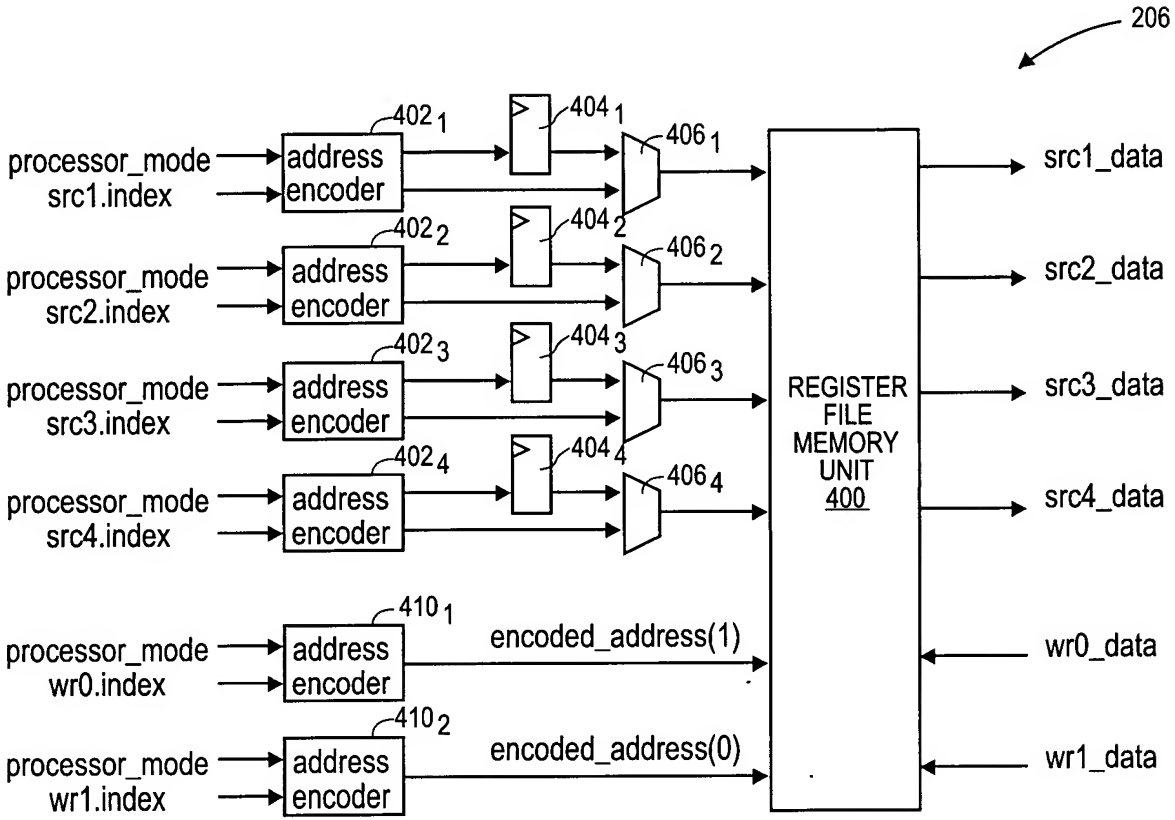
206
processor_mode
src1.index
address
encoder
402 1
404 1
406 1
processor_mode
src2.index
address
encoder
402 2
404 2
406 2
processor_mode
src3.index
address
encoder
402 3
404 3
406 3
processor_mode
src4.index
address
encoder
402 4
404 4
406 4
REGISTER
FILE
MEMORY
UNIT
400
src1_data
src2_data
src3_data
src4_data
processor_mode
wr0.index
address
encoder
410 1
encoded_address(1)
wr0_data
processor_mode
wr1.index
address
encoder
410 2
encoded_address(0)
wr1_data

FIG. 4

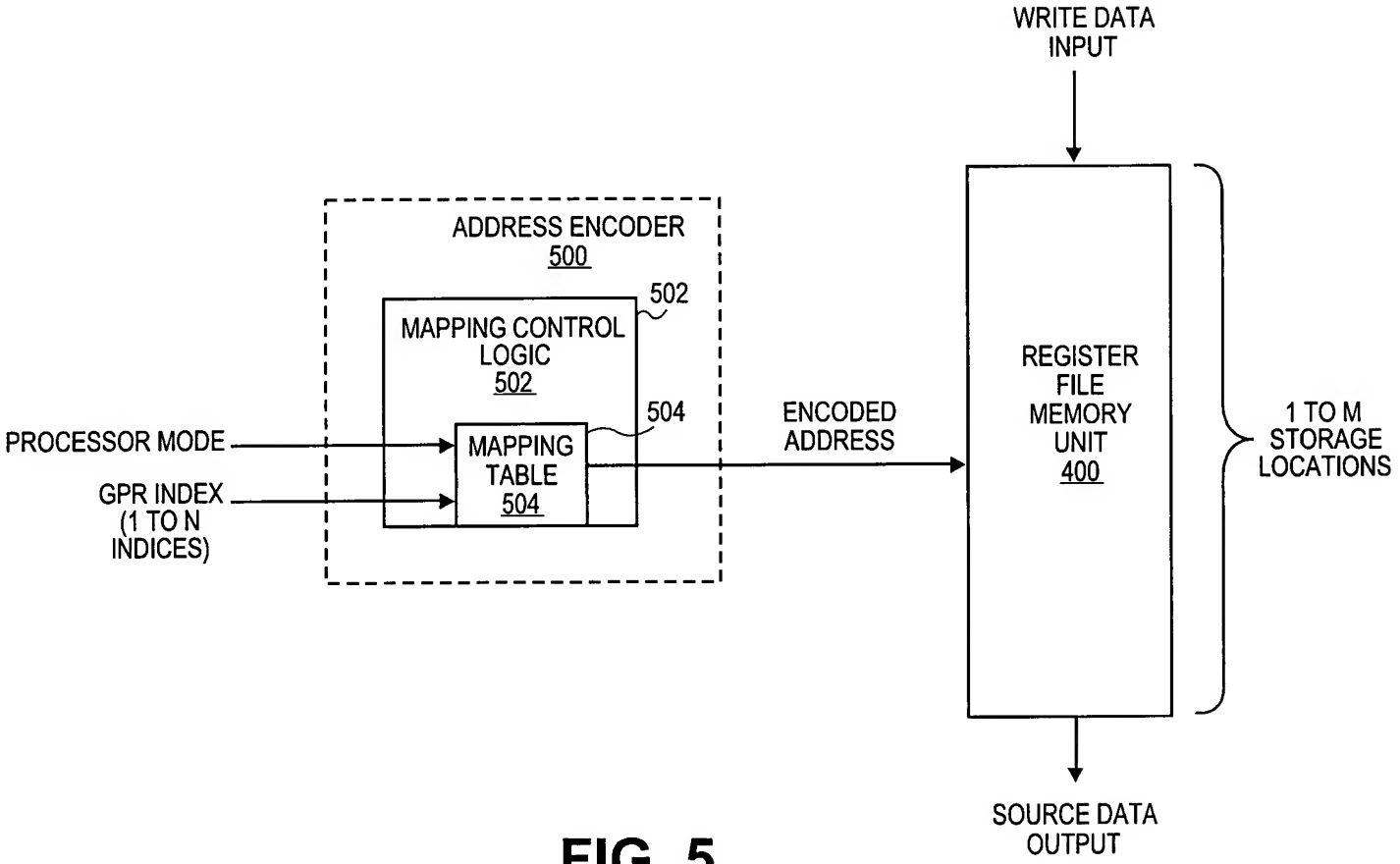
WRITE DATA INPUT
ADDRESS ENCODER
500
502
MAPPING CONTROL LOGIC
502
504
MAPPING TABLE
504
PROCESSOR MODE
GPR INDEX (1 TO N INDICES)
ENCODED ADDRESS
REGISTER FILE MEMORY UNIT
400
1 TO M STORAGE LOCATIONS
SOURCE DATA OUTPUT

FIG. 5

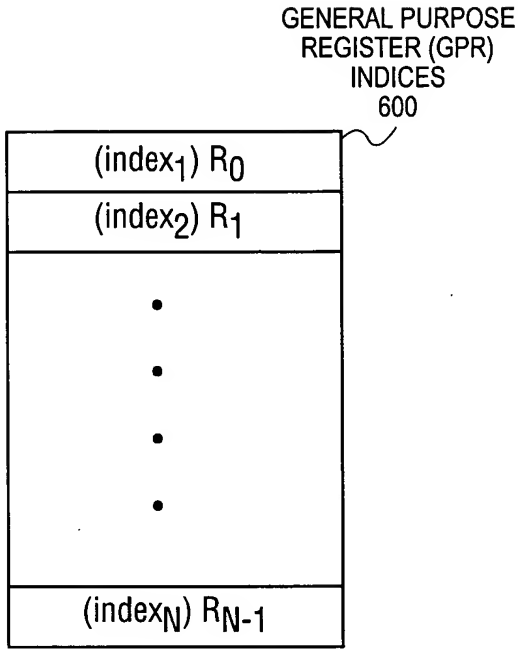
GENERAL PURPOSE
REGISTER (GPR)
INDICES
600
(index1) R0
(index2) R1
(indexN) RN-1

FIG. 6

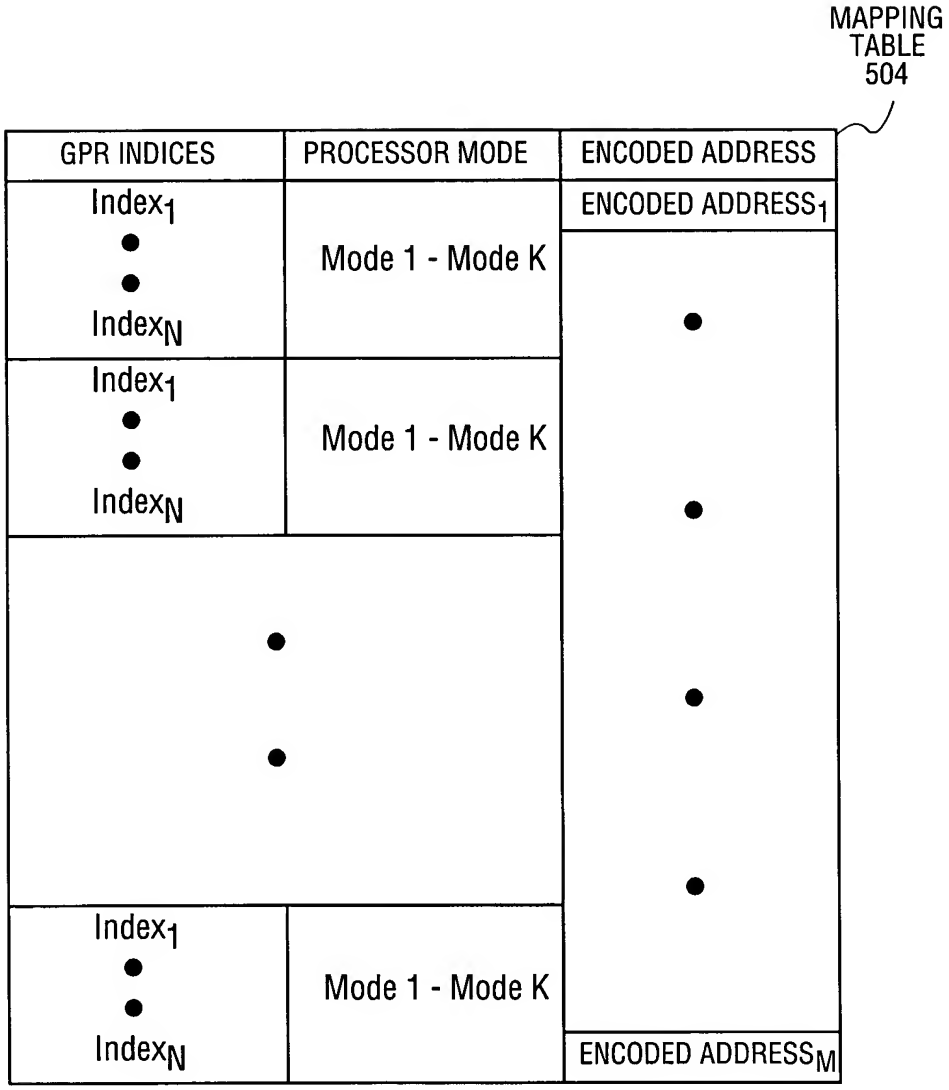
MAPPING TABLE 504
GPR INDICES
PROCESSOR MODE
ENCODED ADDRESS
Index1
IndexN
Mode 1 - Mode K
ENCODED ADDRESS1
Index1
IndexN
Mode 1 - Mode K
Index1
IndexN
Mode 1 - Mode K
ENCODED ADDRESSM

FIG. 7

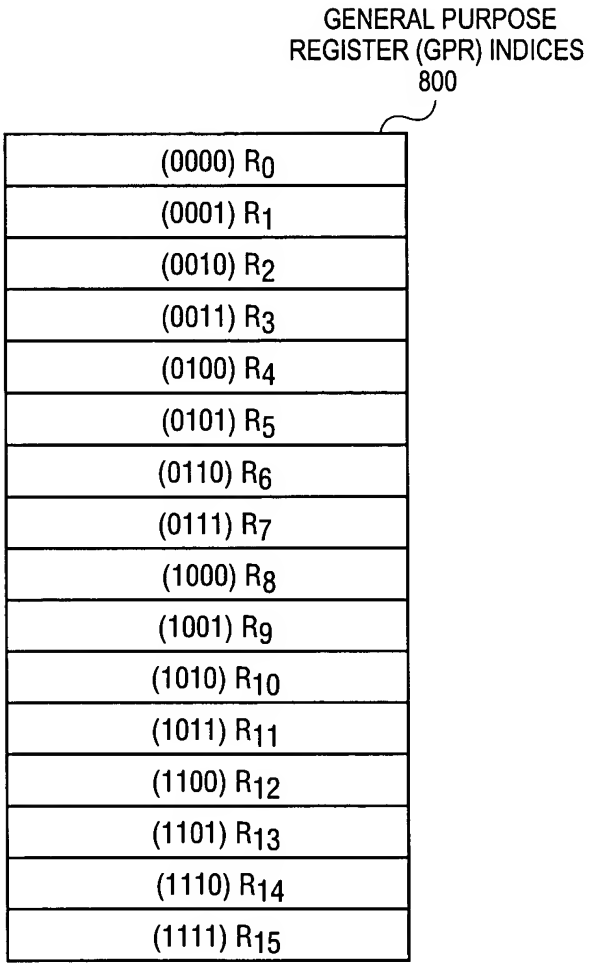
GENERAL PURPOSE
REGISTER (GPR) INDICES
800
(0000) R_0
(0001) R_1
(0010) R_2
(0011) R_3
(0100) R_4
(0101) R_5
(0110) R_6
(0111) R_7
(1000) R_8
(1001) R_9
(1010) R_{10}
(1011) R_{11}
(1100) R_{12}
(1101) R_{13}
(1110) R_{14}
(1111) R_{15}

FIG. 8

MAPPING TABLE 904

GPR Indices (Registers)	Processor Mode	Encoded Address (memory location)
(0000) R_0	MODES 1-N	00000
(0001) R_1		00001
(0010) R_2		00010
(0011) R_3		00011
(0100) R_4		00100
(0101) R_5		00101
(0110) R_6		00110
(0111) R_7		00111
(1000) R_8	MODE 1	01000
(1001) R_9		01001
(1010) R_{10}		01010
(1011) R_{11}		01011
(1100) R_{12}		01100
(1101) R_8	MODE 2	01101
(1110) R_9		01110
(1111) R_{10}		01111
(1110) R_{11}		10000
(1100) R_{12}		10001
(1100) R_{15}	MODE 3	10011
(1110) R_{14}		10010
(1100) R_{13}		10011
(1110) R_{14}	MODE 4	10100
(1100) R_{13}		10101
(1110) R_{14}	MODE 5	10110
(1100) R_{13}		10111
(1000) R_8	MODE N	11000
(1001) R_9		11001
(1010) R_{10}		11010
(1011) R_{11}		11011
(1100) R_{12}		11100
(1101) R_{13}		11101
(1110) R_{14}		11110
(1111) R_{15}		11111

FIG. 9

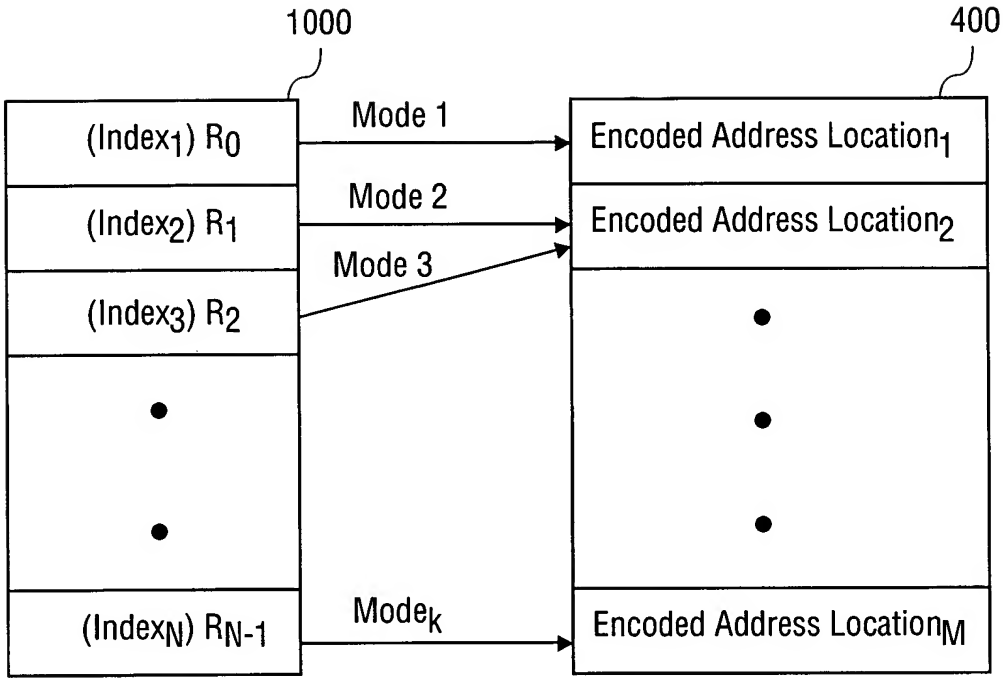

FIG. 10A

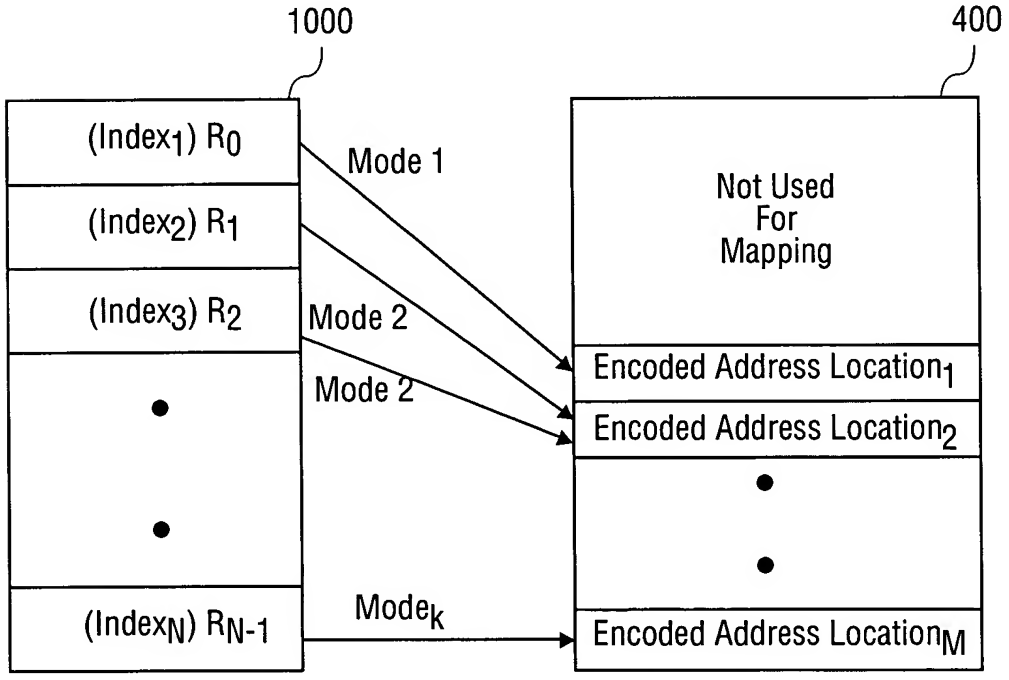

FIG. 10B

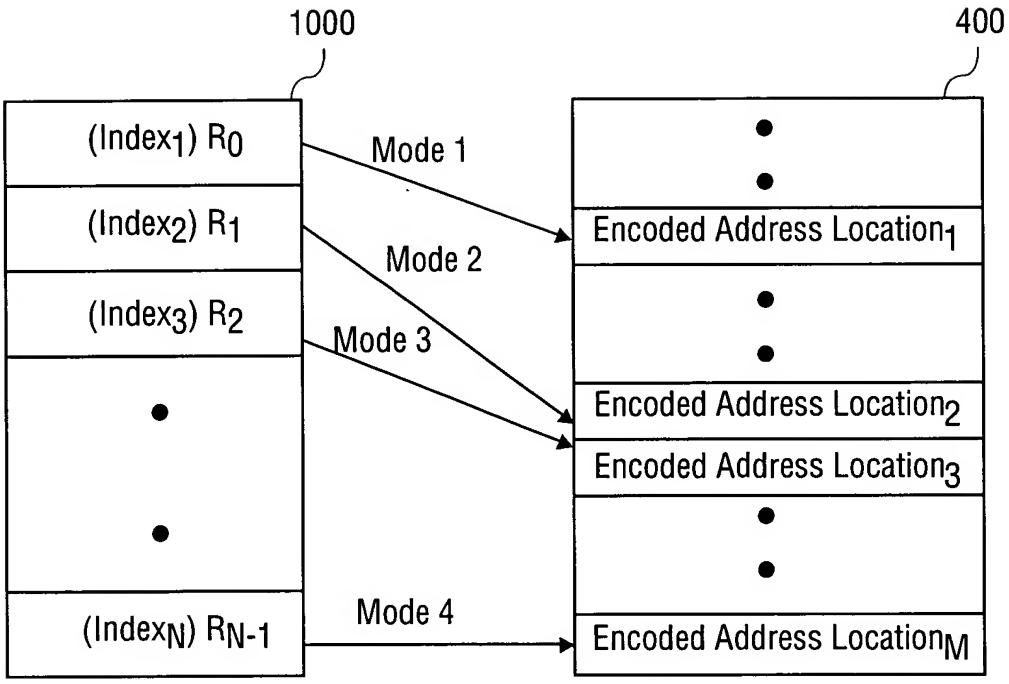
1000
400
(Index1) R0
(Index2) R1
(Index3) R2
(IndexN) RN-1
Mode 1
Mode 2
Mode 3
Mode 4
Encoded Address Location1
Encoded Address Location2
Encoded Address Location3
Encoded Address LocationM

FIG. 10C

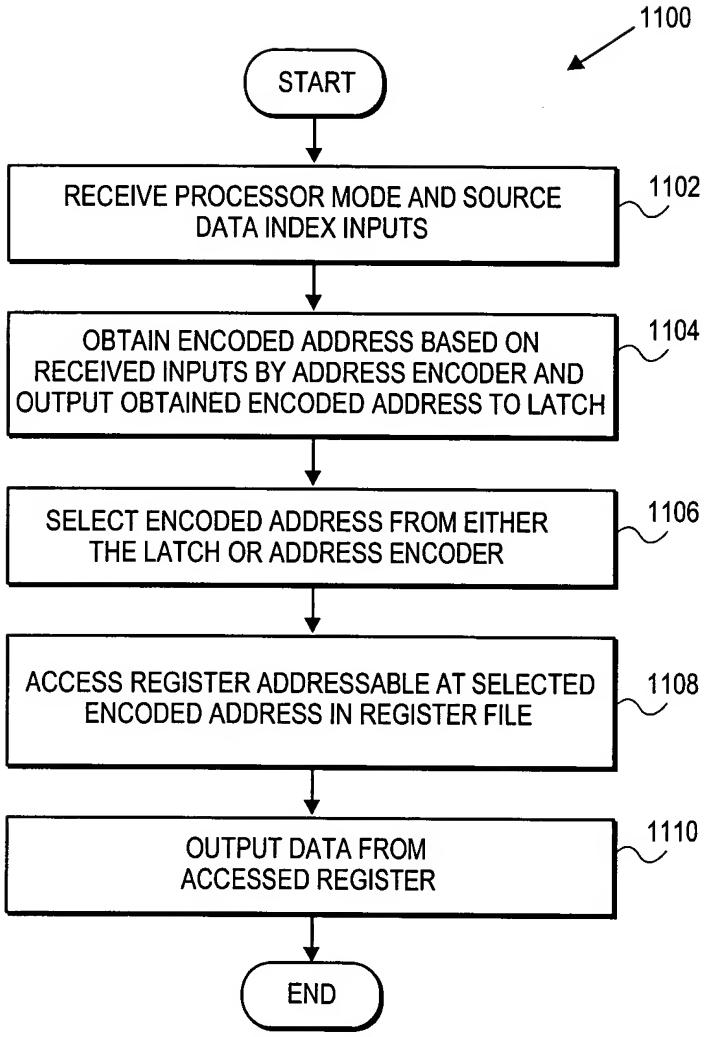
1100
START
RECEIVE PROCESSOR MODE AND SOURCE DATA INDEX INPUTS
1102
OBTAIN ENCODED ADDRESS BASED ON RECEIVED INPUTS BY ADDRESS ENCODER AND OUTPUT OBTAINED ENCODED ADDRESS TO LATCH
1104
SELECT ENCODED ADDRESS FROM EITHER THE LATCH OR ADDRESS ENCODER
1106
ACCESS REGISTER ADDRESSABLE AT SELECTED ENCODED ADDRESS IN REGISTER FILE
1108
OUTPUT DATA FROM ACCESSED REGISTER
1110
END

FIG. 11

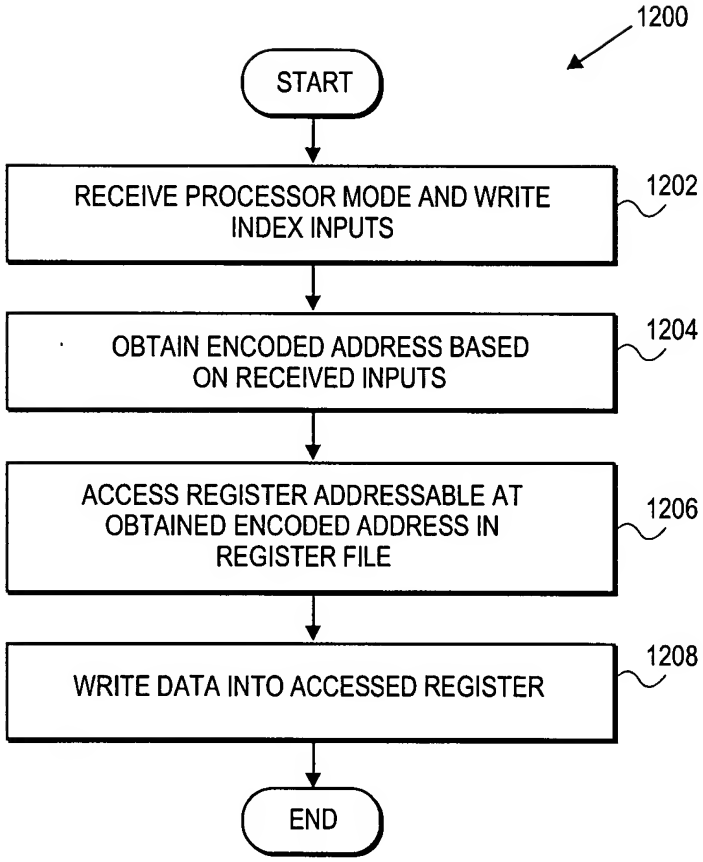
1200
START
RECEIVE PROCESSOR MODE AND WRITE INDEX INPUTS
1202
OBTAIN ENCODED ADDRESS BASED ON RECEIVED INPUTS
1204
ACCESS REGISTER ADDRESSABLE AT OBTAINED ENCODED ADDRESS IN REGISTER FILE
1206
WRITE DATA INTO ACCESSED REGISTER
1208
END

FIG. 12